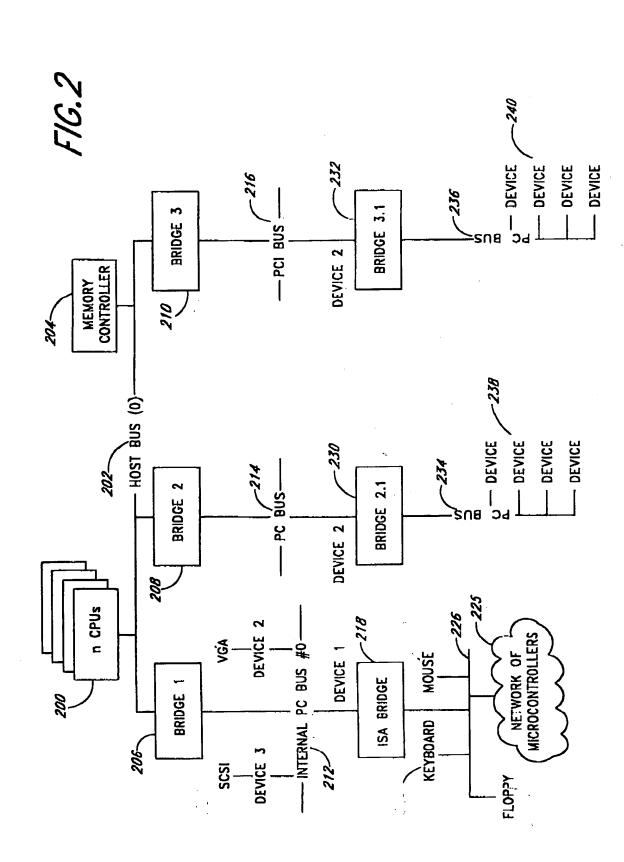
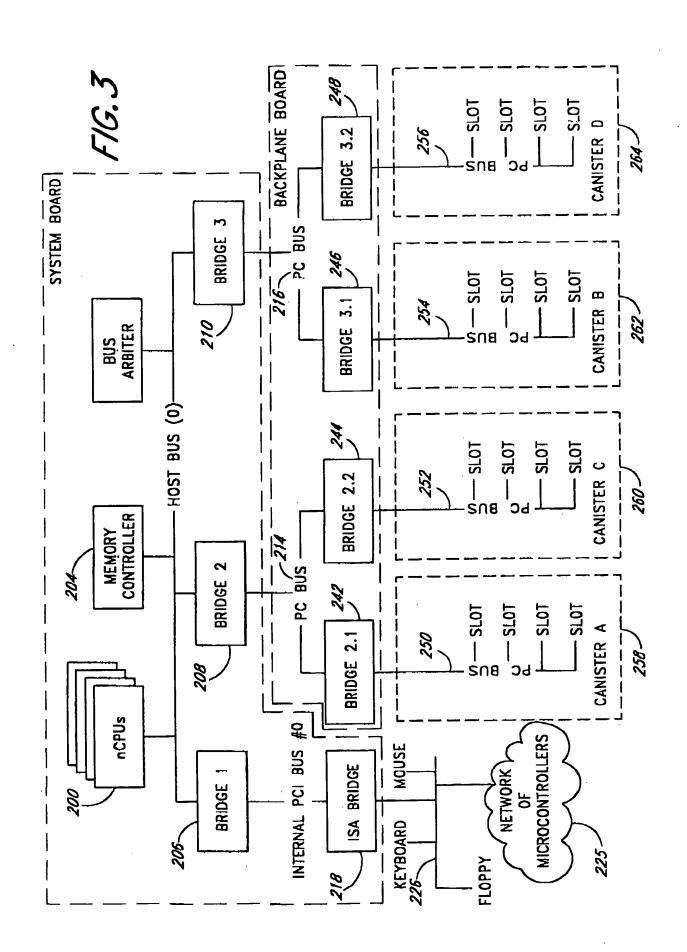
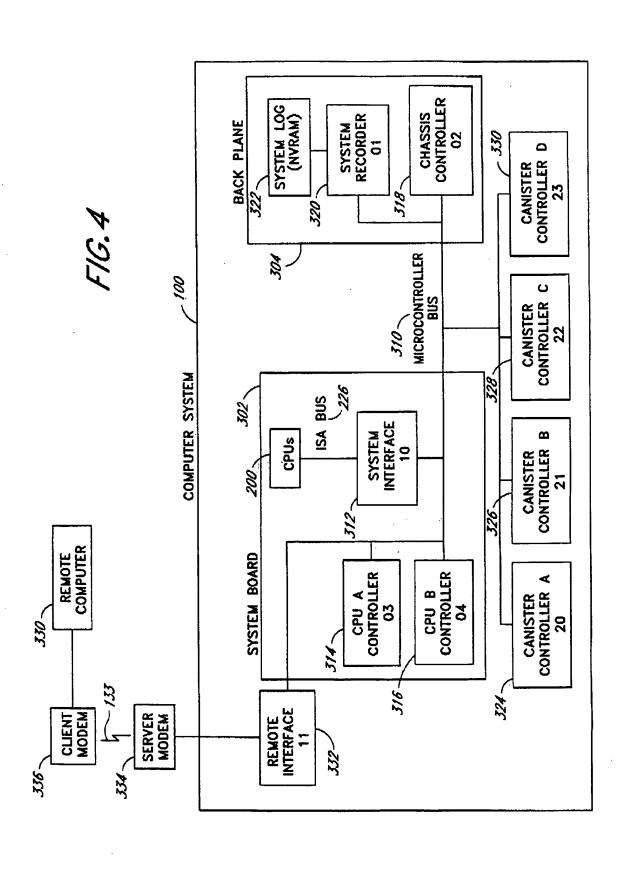
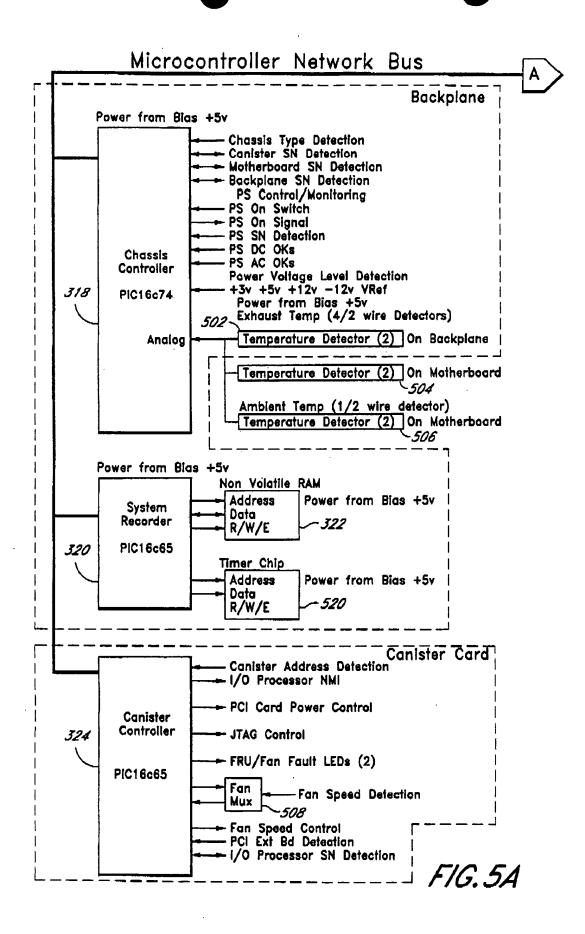


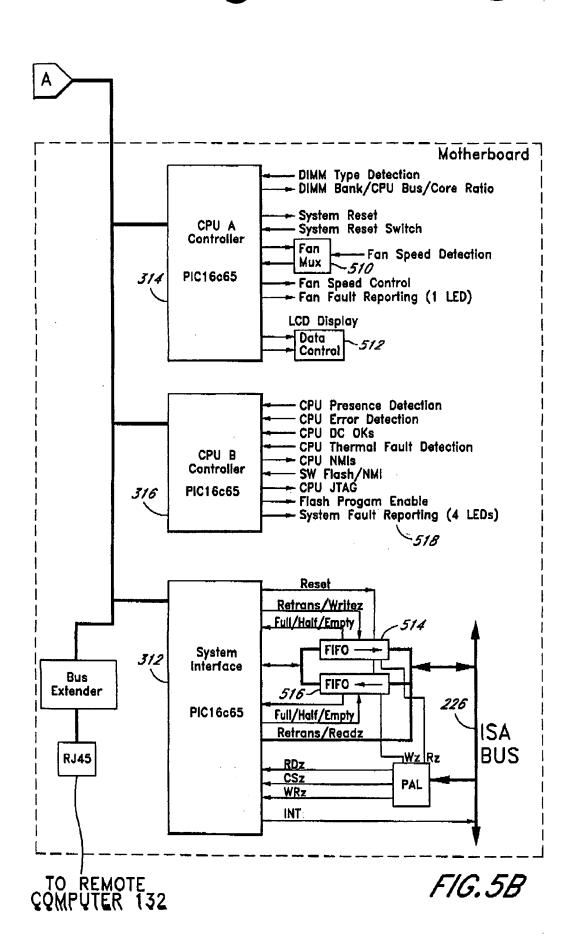
FIG. 1

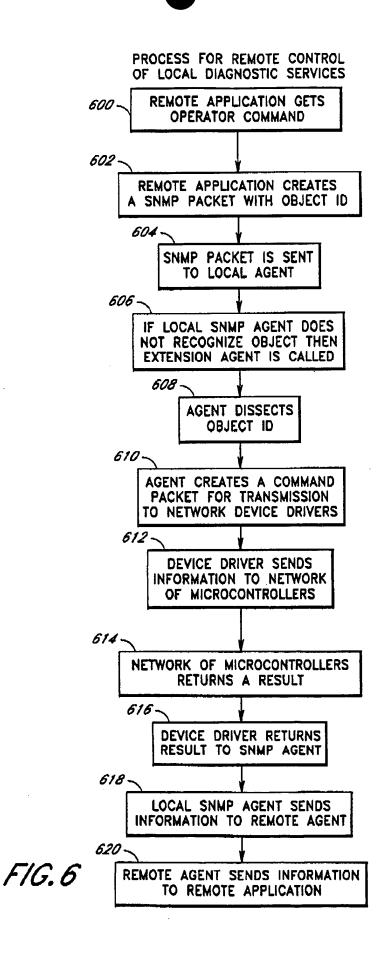


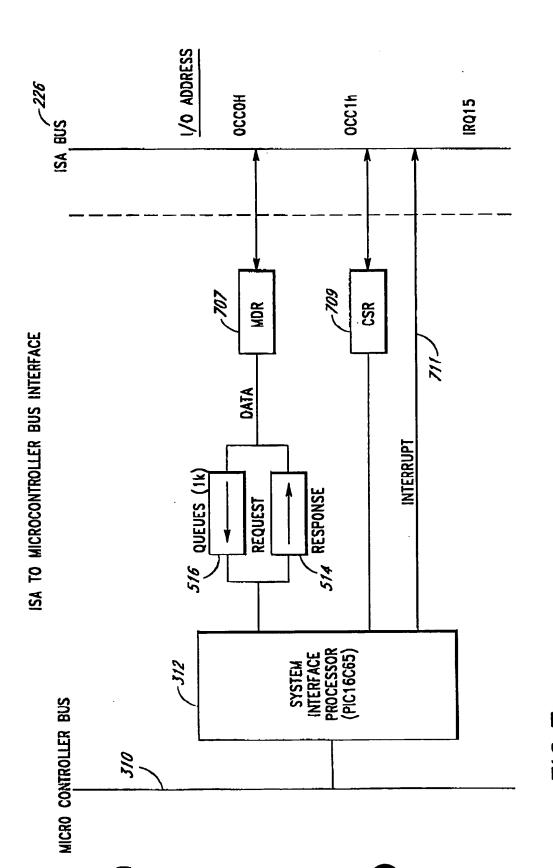






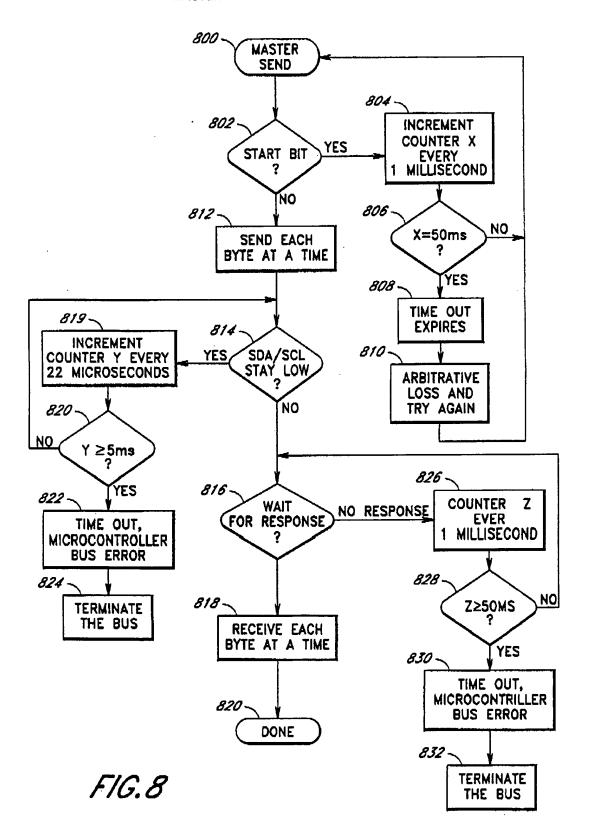


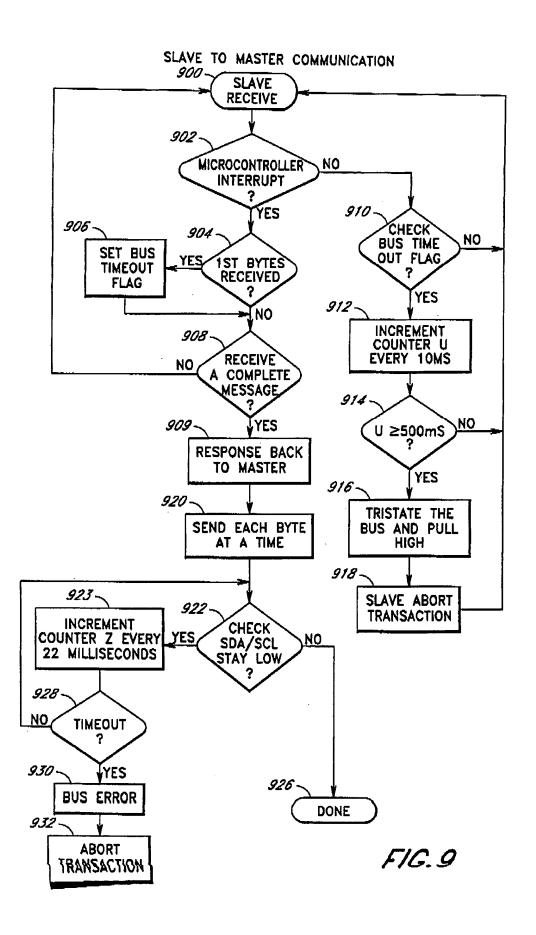


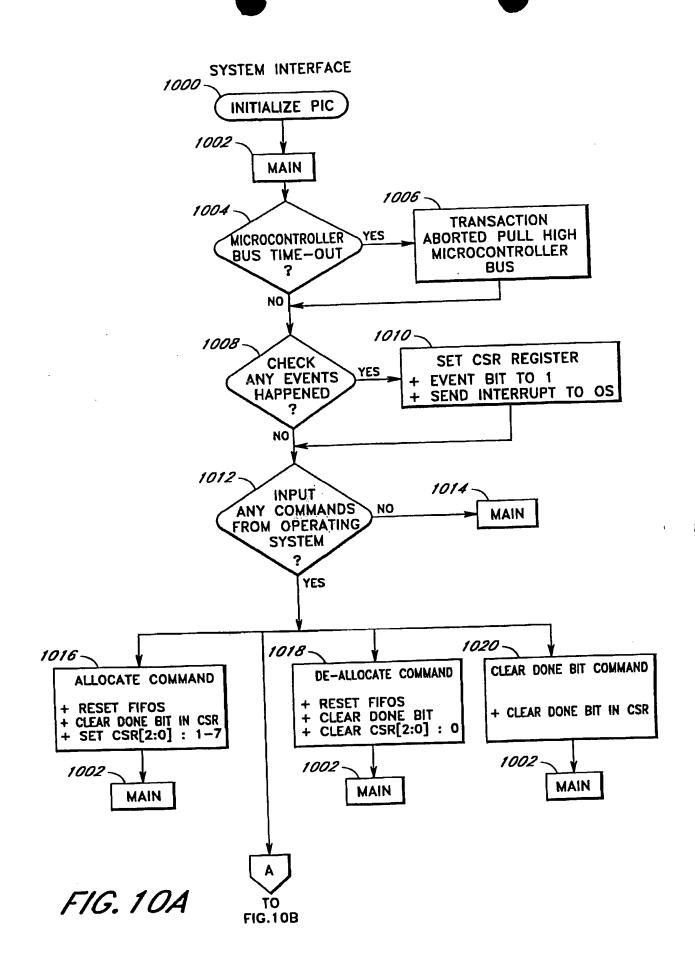


F1G. 7

MASTER TO SLAVE COMMUNICATION

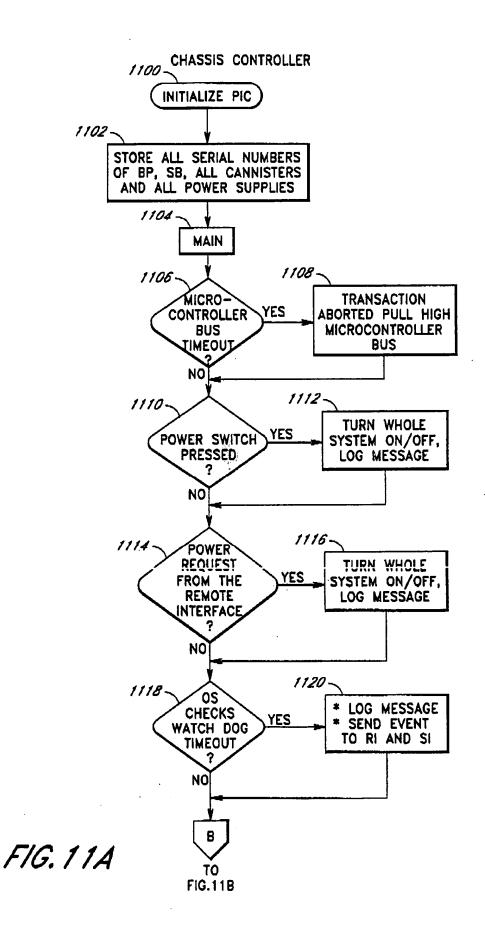




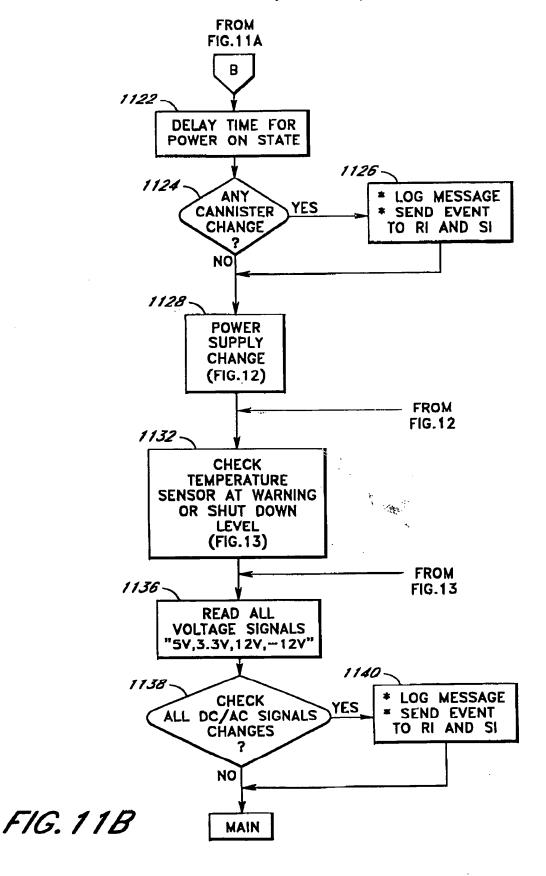


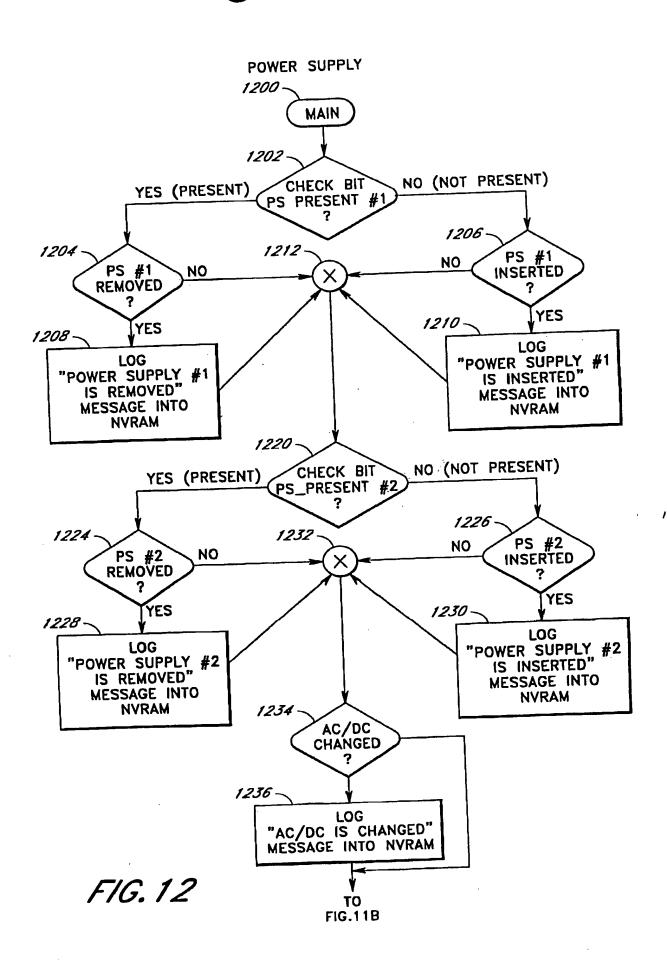
SYSTEM INTERFACE (CONTINUED) **FROM** FIG.10A 1026 -1024-1022 -DISABLE INTERRUPT COMMAND CLEAR INTERRUPT REQUEST ENABLE INTERRUPT COMMAND COMMAND + CLEAR INTERRUPT + CLEAR INTERRUPT + SET INTERRUPT ENABLE REQUEST BIT IN CSR ENABLE BIT IN CSR BIT IN CSR 1002 -1002 -1002 -MAIN MAIN MAIN 1028 -MESSAGE COMMAND + GET DATA FROM FIFO 1032 -1030 -READ/WRITE INTERNAL YES MATCHED FUNCTION COMMAND ADDRESS NO 1034 -SEND COMMAND DATA INTO MICROCONTROLLER BUS TO COMMUNICATE WITH ANOTHER PIC 1002-MAIN

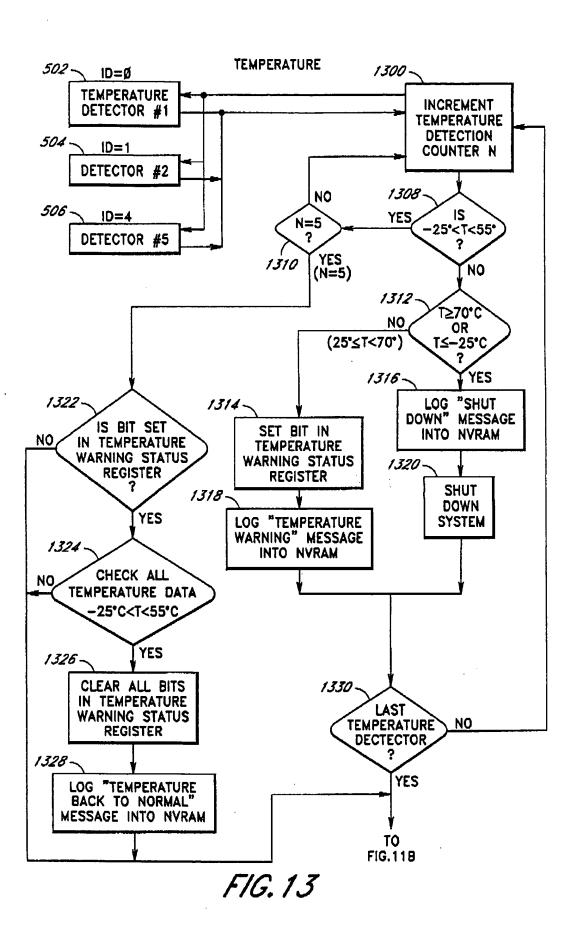
FIG. 10B

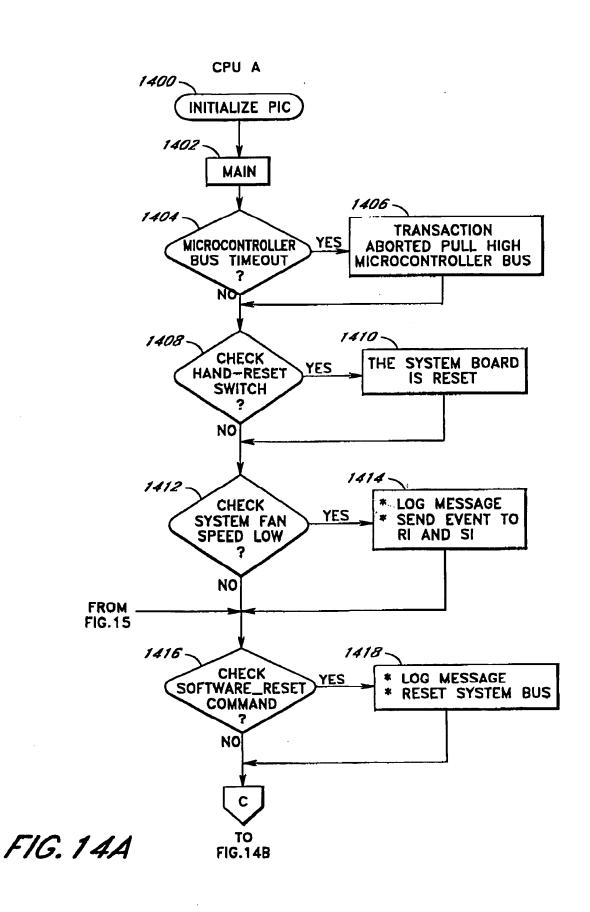


CHASSIS CONTROLLER (CONTINUED)









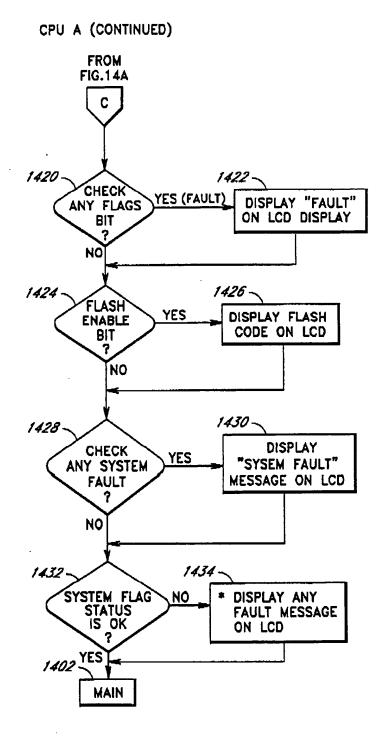
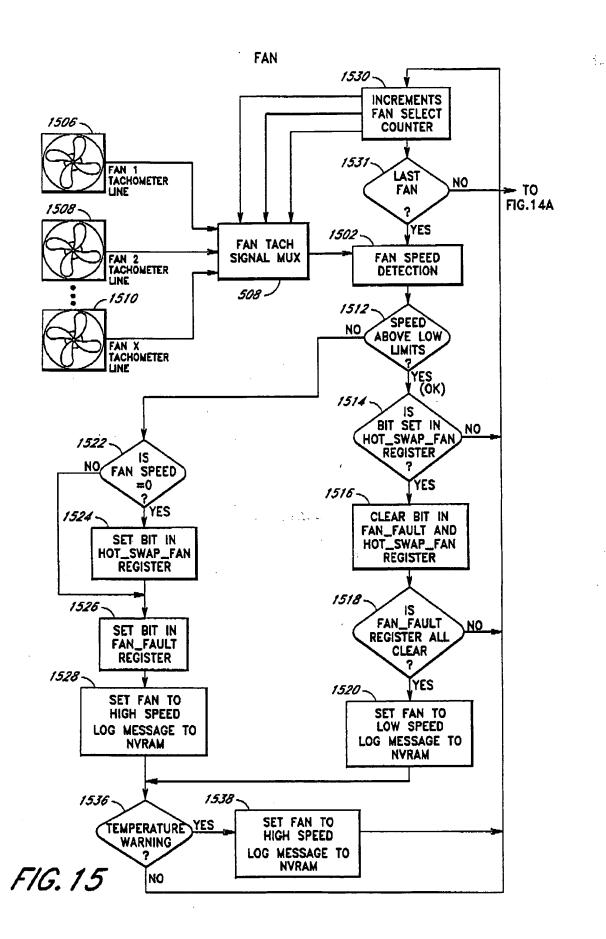
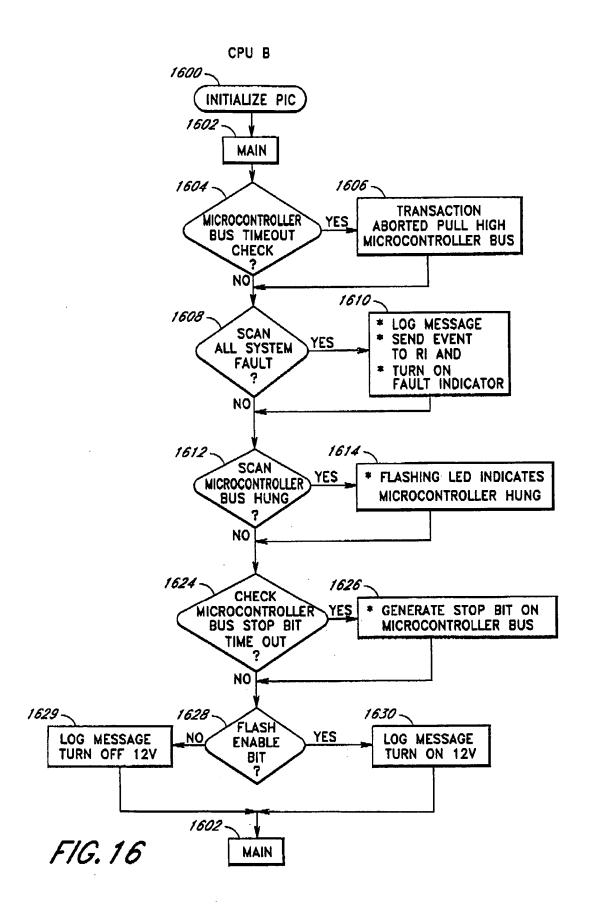


FIG. 14B





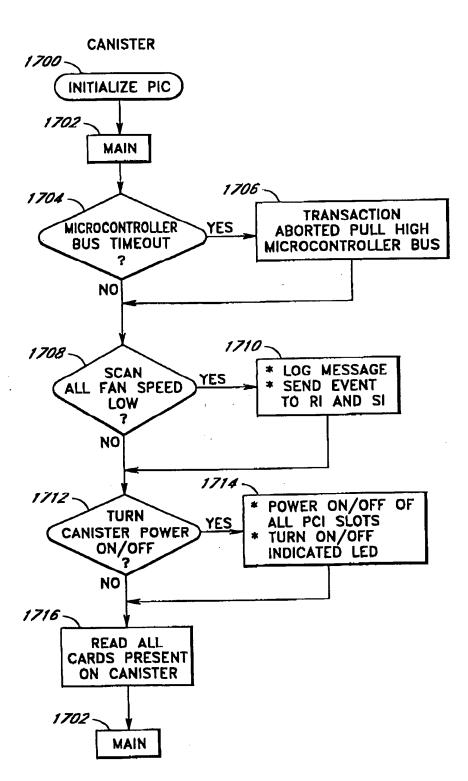


FIG. 17

SYSTEM RECORDER

1

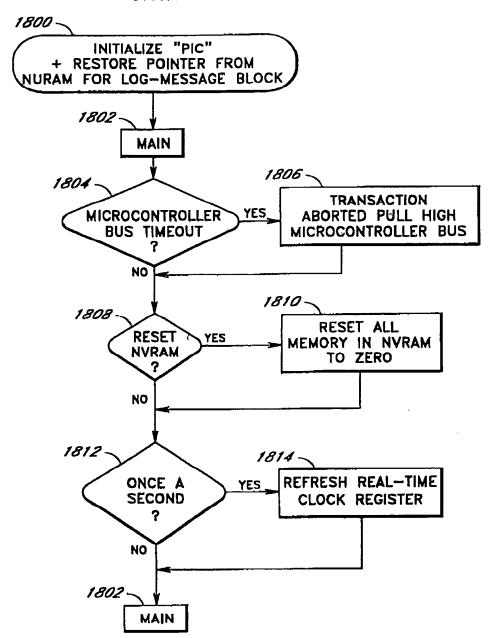


FIG. 18